Notice of Allowability	Application No.	Applicant(s)	
	10/681,244	BAUMER ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/29/2007*.

2. ☒ The allowed claim(s) is/are *1-37 and 41-53, which are renumbered as 1-50*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/31/2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Cynthia Britt/
Primary Examiner
AU 2117 1/4/08

Allowable Subject Matter

1. Claims 1-37 and 41-53 are allowed.

2. Claims 38-40 are cancelled.

3. Applicants' Request for Continued Examination (RCE) and an amendment to the claims filed on 10/29/2007 have been entered.

4. The following is an examiner's statement of reasons for allowance:

The present invention generally relates to serializer/de-serializer integrated circuits with multiple high-speed data ports, and more particularly to a serializer/de-serializer chip that includes the functionality to switch between multiple high-speed data ports.

The claimed invention in claim 1 recites features such as:"...a substrate; a plurality of data ports disposed on the substrate; and an integrated packet bit error rate tester disposed on the substrate for testing a channel coupled to one of the plurality of data ports, including a packet transmit circuit including a first memory for storing transmit bit error rate test packet data, wherein the packet transmit circuit is coupled to the channel under test; a packet receive circuit including a second memory for storing received packet compare data and coupled to the channel under test; and an interface for programming the packet transmit circuit and the packet receive circuit; wherein said packet transmit circuit and said packet receive circuit are deposited on said substrate; wherein the packet transmit circuit generates an arbitrary packet pattern in response to a command from the interface; and wherein the packet receive circuit determines a bit error rate of the channel under test."

The prior art of record Pierson (US 2003/0048781 A1) teaches a system and method for moving voice telephone calls through a data network. More particularly, the system and method are directed to the efficient operation of using identification numbers to route data packets through a communications node without reformatting individual data packets to the native protocol of that communications node (abstract, Pierson).

Butler et al. (US 6,438,717 B1) teach a high speed link between chips and comprising a multiplicity of synchronous serial data channels includes an onboard detector for detecting an error rate for each channel (abstract, Butler et al.). However Butler et al. do not teach that the packet transmit circuit and the

packet receive circuit are deposited on the substrate and the packet transmit circuit generates an arbitrary packet pattern in response to a command from the interface (abstract, Butler et al.).

Rich, III (US 4,967,201) teaches that a microwave transmit/receive module comprises a single multi-layer substrate having at least two opposed mounting surfaces. The substrate including a plurality of integrated dielectric layers, electrical conductors and thermal conductors selectively interconnected between the layers of the substrate (abstract, Rich, III).

Hillman et al. (US 6,140,956) teach a system which tracks and monitors a vehicle by utilizing cellular communication componentry and global positioning system componentry is disclosed. The system provides for simultaneous and continuous transmission of a voice signal and location data to a monitoring center (abstract, Hillman et al.).

Morikawa (US 2002/0054569 A1) teaches that in carrying out data communication by use of a communication network where accounting is made according to a data amount, the start and end of transmission/reception of a set of objective data to be transmitted/received are recognized, and the amount of packets transmitted/received from the start to the end of transmission/reception of the set of objective data to be transmitted/received is measured, and thereby a communication charge is calculated (abstract, Morikawa).

Chen et al. (US 5,726,991) teach a data communication method and apparatus includes an integral bit error rate test system. The system is adapted to receive digital data signals to be transmitted over a communication link and includes a transmitter for transmitting the data signals onto the link (abstract, Chen et al.).

Yu (US 2001/0012288 A1) teaches a data transmission apparatus and method for transmitting data between physical layer side device and network layer device, which encapsulating a novel LAPS framing-de-framing into SPE/VC of a HDLC-like frame using a variable SAPI value (abstract, Yu).

Mejia et al. (US 2003/0009307 A1) teach pattern detection methods and arrangements for monitoring a Fibre Channel, a Gigabit Ethernet, or other like data stream for programmable trigger patterns (abstract, Mejia et al.).

Ghuman et al. (US 6,081,570) teach a parallel integrated frame synchronizer which implements a sequential pipeline process wherein serial data in the form of telemetry data or weather satellite data enters the synchronizer by means of a front-end subsystem and passes to a parallel correlator subsystem or a weather satellite data processing subsystem (abstract, Ghuman et al.).

However the prior arts of record do not teach a substrate; a plurality of data ports disposed on the substrate; and an integrated packet bit error rate tester disposed on the substrate for testing a channel coupled to one of the plurality of data ports, including a packet transmit circuit including a first memory for storing transmit bit error rate test packet data, wherein the packet transmit circuit is coupled to the channel under test; a packet receive circuit including a second memory for storing received packet compare data and coupled to the channel under test; and an interface for programming the packet transmit circuit and the packet receive circuit; wherein said packet transmit circuit and said packet receive circuit are deposited on said substrate; wherein the packet transmit circuit generates an arbitrary packet pattern in response to a command from the interface; and wherein the packet receive circuit determines a bit error rate of the channel under test.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 1 is allowable over the prior arts of record. Claims 2-23 are allowed because of the combination of additional limitations and the limitations listed above.

- Claim 24 recites similar features as in claim 1. Thus claim 24 is allowable over the prior arts of record. Claims 25-37 are allowed because of the combination of additional limitations and the limitations listed above.
- The claimed invention in claim 41 recites features such as:"...a method of testing a bit error rate of a channel coupled to a transmitter memory that is part of an integrated circuit deposited on a substrate and to a receiver that is part of the integrated circuit deposited on the substrate, comprising: generating a test packet including an arbitrary marker pattern; loading the test packet into the transmitter memory in the integrated circuit; transmitting the test packet from the transmitter memory over the channel; capturing a received test packet from the channel coupled

to the integrated circuit; and determining the bit error rate of the channel based on the received test packet."

The prior art of record Pierson (US 2003/0048781 A1) teaches a system and method for moving voice telephone calls through a data network. More particularly, the system and method are directed to the efficient operation of using identification numbers to route data packets through a communications node without reformatting individual data packets to the native protocol of that communications node (abstract, Pierson).

Butler et al. (US 6,438,717 B1) teach a high speed link between chips and comprising a multiplicity of synchronous serial data channels includes an onboard detector for detecting an error rate for each channel (abstract, Butler et al.). However Butler et al. do not teach that a transmitter and a receiver are part of an integrated circuit deposited on a substrate and generating a test packet including an arbitrary marker pattern (abstract, Butler et al.).

Rich, III (US 4,967,201) teaches that a microwave transmit/receive module comprises a single multi-layer substrate having at least two opposed mounting surfaces. The substrate including a plurality of integrated dielectric layers, electrical conductors and thermal conductors selectively interconnected between the layers of the substrate (abstract, Rich, III).

Hillman et al. (US 6,140,956) teach a system which tracks and monitors a vehicle by utilizing cellular communication componentry and global positioning system componentry is disclosed. The system provides for simultaneous and continuous transmission of a voice signal and location data to a monitoring center (abstract, Hillman et al.).

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Chen et al. (US 5,726,991) teach a data communication method and apparatus includes an integral bit error rate test system. The system is adapted to receive digital data signals to be transmitted over a communication link and includes a transmitter for transmitting the data signals onto the link (abstract, Chen et al.).

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However the prior arts of record do not teach a method of testing a bit error rate of a channel coupled to a transmitter memory that is part of an integrated circuit deposited on a substrate and to a receiver that is part of the integrated circuit deposited on the substrate, comprising: generating a test packet including an arbitrary marker pattern; loading the test packet into the transmitter memory in the integrated circuit; transmitting the test packet from the transmitter memory over the channel; capturing a received test packet from the channel coupled to the integrated circuit; and determining the bit error rate of the channel based on the received test packet.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 41 is allowable over the prior arts of record. Claims 42-53 are allowed because of the combination of additional limitations and the limitations listed above.

- Thus claims 1-37 and 41-53 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Patent Examiner

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Primary Examiner
AU 2117 1/4/08